Notice of Allowability	Application No. 09/834,342	Applicant(s) LAHIRI ET AL.	
	Examiner Fred Ferris	Art Unit 2128	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address--

All claims being allowable, PROSECUTION ON THE MERITS IS (OR REMAINS) CLOSED in this application. If not included herewith (or previously mailed), a Notice of Allowance (PTOL-85) or other appropriate communication will be mailed in due course. **THIS NOTICE OF ALLOWABILITY IS NOT A GRANT OF PATENT RIGHTS.** This application is subject to withdrawal from issue at the initiative of the Office or upon petition by the applicant. See 37 CFR 1.313 and MPEP 1308.

1. ☒ This communication is responsive to *14 March 2005*.

2. ☒ The allowed claim(s) is/are *1-8,11 and 13-20*, now renumbered as 1-17.

3. ☒ The drawings filed on *13 April 2001* are accepted by the Examiner.

4. ☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).
   a) ☐ All b) ☐ Some* c) ☐ None of the:
      1. ☐ Certified copies of the priority documents have been received.
      2. ☐ Certified copies of the priority documents have been received in Application No. _____ .
      3. ☐ Copies of the certified copies of the priority documents have been received in this national stage application from the International Bureau (PCT Rule 17.2(a)).

   * Certified copies not received: _____.

Applicant has THREE MONTHS FROM THE "MAILING DATE" of this communication to file a reply complying with the requirements noted below. Failure to timely comply will result in ABANDONMENT of this application.
THIS THREE-MONTH PERIOD IS NOT EXTENDABLE.

5. ☐ A SUBSTITUTE OATH OR DECLARATION must be submitted. Note the attached EXAMINER'S AMENDMENT or NOTICE OF INFORMAL PATENT APPLICATION (PTO-152) which gives reason(s) why the oath or declaration is deficient.

6. ☐ CORRECTED DRAWINGS (as "replacement sheets") must be submitted.
   (a) ☐ including changes required by the Notice of Draftsperson's Patent Drawing Review (PTO-948) attached
      1) ☐ hereto or 2) ☐ to Paper No./Mail Date _____.
   (b) ☐ including changes required by the attached Examiner's Amendment / Comment or in the Office action of Paper No./Mail Date _____.

   Identifying indicia such as the application number (see 37 CFR 1.84(c)) should be written on the drawings in the front (not the back) of each sheet. Replacement sheet(s) should be labeled as such in the header according to 37 CFR 1.121(d).

7. ☐ DEPOSIT OF and/or INFORMATION about the deposit of BIOLOGICAL MATERIAL must be submitted. Note the attached Examiner's comment regarding REQUIREMENT FOR THE DEPOSIT OF BIOLOGICAL MATERIAL.

Attachment(s)

1. ☒ Notice of References Cited (PTO-892)
2. ☐ Notice of Draftperson's Patent Drawing Review (PTO-948)
3. ☐ Information Disclosure Statements (PTO-1449 or PTO/SB/08), Paper No./Mail Date _____
4. ☐ Examiner's Comment Regarding Requirement for Deposit of Biological Material
5. ☐ Notice of Informal Patent Application (PTO-152)
6. ☐ Interview Summary (PTO-413), Paper No./Mail Date _____ .
7. ☐ Examiner's Amendment/Comment
8. ☒ Examiner's Statement of Reasons for Allowance
9. ☐ Other _____.

DETAILED ACTION

1. Claims 1-27 have been presented for examination based on applicant's amendment filed 14 March 2005. Applicants have cancelled claims 9-10, 12, and 21-27. Claims 13-19 were previously allowed over the prior art of record. Amended claims 1-8, 11 and 20 have now been allowed over the prior art of record.

Response to Arguments

2. Applicant's arguments filed 14 March 2005 with respect to amended claims 1-8, 11, and 20 have been fully considered and are persuasive. The 35 USC 102(b) rejection is now withdrawn.

Allowable Subject Matter

3. Claims 1-8, 11, 13-19, and 20 are allowed over the prior art of record.

The following is an examiner's statement of reasons for allowance:

Applicants are disclosing a method and system for simulating the performance of a segmented cache memory of various sizes by applying data references to the simulated cache, storing the references in a trace buffer, calculating the number or "hits" or "misses" to the segments, and generating a performance estimate. This has been disclosed in the prior art. The prior art of record, while generally disclosing these features, does not meet the conditions as suggested in MPEP section 2132, namely:

"The identical invention must be shown in as complete detail as is contained in the ... claim." Richardson v. Suzuki Motor Co., 868 F.2d 1226, 1236, 9 USPQ2d 1913,

1920 (Fed. Cir. 1989). The elements must be arranged as required by the claim, but this is not an ***ipsissimis verbis*** *test, i.e., identity of terminology is not required.* ***In re Bond,*** *910 F.2d 831, 15 USPQ2d 1566 (Fed. Cir. 1990)."*

In particular, the prior art of record does not disclose the specific sequence of steps and the arrangement of elements relating to generating an estimate of cache performance, via a multi-segmented cache simulator, using references received during operation of database management system, as required by independent claim 13, or, the use of a correction factor by applying data references to the operational data cache to an initial miss rate in a second simulated cache, in multiple caches, where the number of buffers matches the number of buffers in the operational cache, as now recited in independent claims 1 and 20.

The closest prior art uncovered during examination discloses the following elements relating to the claimed invention:

- *U.S. Patent 5,940,618 issued to Blandy et al: discloses a cache simulator and performance evaluation.*
- *"Trace-Driven Memory Simulation: A Survey", R.A. Uhlig et al, ACM Computing Surveys, Vol. 29, No. 2, June 1997: discloses trace based cache simulation techniques and performance of commercially available cache simulators.*
- *"Automatic and Efficient Evaluation of Memory Hierarchies for Embedded Systems", S. Abraham et al, Hewlett-Packard # HPL-1999-132, October*

1999: discloses trace based cache simulation techniques and performance of the commercially available "Cheetah" simulator.

- *"Active Memory: A New Abstraction for Memory system Simulation", A.R. Lebeck et al, ACM Transactions on Modeling and Computer Simulation, Vol. 7, No. 1, January 1997: discloses fast-cache, trap-driven and trace based cache simulation techniques and performance of the commercially available simulators.*
- *"Retargetable Cache Simulation Using High Level Processor Models", R. Ravindran et al, IEEE 0-7695-0954-1/01, IEEE January 2001: discloses re-targetable cache simulation techniques and performance of the commercially available "Cheetah" simulator.*

These references generally disclose features relating to cache performance improvement using cache simulators. However, the prior art of record does not disclose specific sequence of steps and the arrangement of elements required by independent claims 1, 13, and 20. Specifically, independent claims 1 and 20 includes limitations relating to the use of a correction factor by applying data references to the operational data cache to an initial miss rate in a second simulated cache, in multiple caches, where the number of buffers matches the number of buffers in the operational cache that is not explicitly disclosed in the prior art of record. Dependent claims 2-8, and 11 are deemed allowable as being dependent from independent claim 1. Independent claim 13 includes limitations relating to storing references during operation of a data base management system, and maintaining a multi-segmented cache simulator with simulated buffers

storing identifiers where the multiple caches include a set of segments that are different from the other caches.

The claimed multi-segmented cache simulator of the present invention is specifically defined by applicant's specification as multi-segments consisting of eight segments of cache simulator (200) that are designated as cache0-cache7 configured to hold 250,000 simulated buffers. (Specification page 9, lines 5-25, page 14, lines 12-27, and in Figs. 2 and 4a – 4b) Claim 13 further includes limitations relating to the sequence of cache simulator steps for stored cache references including; searching a first buffer for referenced data item and, if in segmented memory increment first buffer hit counter & move reference to segment head, if not, increment miss counter & store identifier in second buffer, then store second buffer at head of cache simulator, and generate an estimate of performance. This specific sequence of steps for generating an estimate of cache performance, via a multi-segmented cache simulator, using references received during operation of database management system, is not explicitly disclosed in the prior art of record. Dependent claims 14-19 are allowable as being dependent from claim 13.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

4. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Fred Ferris whose telephone number is 571-272-3778 and whose normal working hours are 8:30am to 5:00pm Monday to Friday. Any inquiry of a general nature relating to the status of this application should be directed to the group receptionist whose telephone number is 571-272-3700. If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Jean Homere can be reached at 571-272-3780. The Official Fax Number is: (703) 872-9306

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JEAN R. HOMERE
PRIMARY EXAMINER